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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/409,940 | 09/30/1999 | BRYAN KEITH BULLIS | RAL9-99-0056 | 6159 |

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| EXAMINER |
|---|
| FERRIS III, FRED O |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

DATE MAILED: 07/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/409,940 | BULLIS ET AL. | |
| | Examiner | Art Unit | |
| | Fred Ferris | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 September 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

*1. Claims 1-23 have been presented for examination. Claims 1-23 have been rejected by the examiner.*

### *Drawings*

*2. The subject matter of this application admits of illustration by a drawing to facilitate understanding of the invention. Applicant is required to furnish a drawing under 37 CFR 1.81. No new matter may be introduced in the required drawing. Specifically, applicants have claimed a "snooper", "generator", "interface, and "checker" process that has not been adequately represented in* ***figures*** *or text. While figures 4a and 4b do incorporate these functions as a "block", each process needs to be represented by a functional flow chart in order to clarify the inventions operation.*

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

*2. Claims 1-23 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*

*Specifically, regarding independent claim 1: Claim 1 is drawn to a system for providing simulation of an integrated circuit consisting of:*

*A **snooper** coupled with **the interface** for obtaining an **output** by the island.*

*A **checker** coupled with **the interface** for checking whether output is **desired output**.*

*A **generator** coupled with **the island** for providing an **input** to the island.*

*The specification of the claimed invention does not adequately disclose the operation of the claimed "**snooper**" or "**the interface**" in a way that would allow one skilled to art to make and/or use it. The specification makes reference to the snooper being "coupled with an interface" and being for "obtaining an output provided by the island during simulation and forwarding the information to the checker" but does not disclose an algorithm or technique for the implementation of either the "snooper" or "the interface".*

*When "snoopers" are used in electronic systems, they are generally realized in either hardware or software. For example, software "snoopers" are can be employed by the resource manager of a communication network for purposes such as the extraction and verification of information relating to ID packets. Hardware "snoopers" are generally comprised of control logic, address sequencer, data sequencer, timing signals, and latch-and-hold circuits, and perform a similar function but are typically used for monitoring and verifying hardware status.*

*If the claimed "snooper" is realized in software, then an algorithm and flow chart of the "snooping" process should be disclosed. If the "snooper" is realized in hardware then a block diagram and hardware description should be provided.*

*The specifics of the claimed "interface" is also not disclosed in the specification. While numerous industry standard electronic interfaces such as RS-232, IEEE-488, VME, etc. do exist, the applicants have not identified a standard interface nor have they disclosed their own design. The specifics of the claimed "interface" appear to be critical matter relating to the operation of the claimed invention and needs to be disclosed in detail.*

*The claimed "checker" is further not disclosed by the specification in a way that would allow one skilled in the art to make and/or use it. The specification references the checker being "coupled with the interface" and that it is for "checking the outputs to determine whether the outputs are desired outputs" but does not disclose how the checker performs the claimed "checking" of the output and does not disclose what constitutes a "desired output".*

*The claimed "generator" is also not disclosed by the specification in a way that would allow one skilled in the art to make and/or use it. Reference is made to the "generator" and being "coupled with an interface for providing inputs or outputs to the island" and usually "directed by a test case, but no description of the interface coupling or the related inputs and outputs is provided. Further, no description or explanation of how the generator is "directed by a test case" is given and there is no description of how the generator actually functions.*

*Dependent claims 2-9 inherit these defects.*

*Regarding independent claim 10: Claim 10 is drawn to a method for providing simulation of an integrated circuit consisting of the steps of:*

***Snooping** the **interface** to obtain an output by the island.*

***Checking** the output to determine whether the **output is desired**.*

***Providing** an input to the island during simulation.*

***Directing** the providing of the input using a **test case.***

*As previously described the specification of the claimed invention does not adequately disclose the operation of the claimed "**snooper**", "**interface**", "**checker**", "**generator**", "**test case direction**", or the related **steps** involved in each process (i.e. "snooping", "checking" etc.) in a way that would allow one skilled to art to make and/or use it. Accordingly, independent claim 10 is rejects as described above.*

*Dependent claims 11-16 inherit these defects.*

*Regarding independent claim 17 and dependent claims 18-23: Claims 17-23 are directed toward the computer readable medium and program instructions for the features outlined in claims 1-16 and are rejected using the reasoning as disclosed above.*

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

*3. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by U.S. Patent 6,175,946 issued to Ly et al.*

*While the specification regarding the claimed invention is delinquent in the areas cited in the 35 U.S.C. 112(1) rejections section of this office action the examiner has made prior art rejections based on the limited scope of information contained in the specification for supporting the claims.*

*Independent claim 1 is drawn to a system for providing* ***simulation*** *of an* ***integrated circuit*** *consisting of:*

*A* ***snooper*** *coupled with* ***the interface*** *for obtaining an* ***output*** *by the island.*

*A* ***checker*** *coupled with* ***the interface*** *for checking whether output is* ***desired output****.*

*A* ***generator*** *coupled with* ***the island*** *for providing an* ***input*** *to the island.*

*Regarding independent claim 1: Ly teaches a system that monitors (**snoops**) the **simulation** of an **integrated circuit** design and is capable of automatically **generating** a **checker** (with **interface**) and flagging defective behavior (for **desired output**) of the circuit in a semiconductor die (containing islands). (Abstract, Summary of Invention, Figs. 1, 2, 5, 6, CL2-L54, CL3-L1-7, CL3-L25, L50, CL25-L52)*

*Ly further teaches that the use of "**snoopers**" to monitor the operation of an integrated circuit simulation is well known. (see CL2-L6)*

*Regarding dependent claims 2-9: Ly teaches a system where the **checker** incorporates and **interface** (**coupled** to) a monitor (**snooper**) and automatic **generator** for use in **integrated circuit** design where the generator and checker are obviously **reusable**. (CL2-L54, CL3-L1-7, CL3-L25, L50, CL25-L52) Ly also teaches that the use a **test case** (golden rule or test vector) in monitoring the operation of an integrated circuit simulation is well known. (see CL2-L18)*

*Independent claim 10 is drawn to a method for providing simulation of an integrated circuit consisting of the steps of:*

***Snooping** the **interface** to obtain an output by the island.*

***Checking** the output to determine whether the **output is desired**.*

***Providing** an input to the island during simulation.*

***Directing** the providing of the input using a **test case.***

*Regarding independent claim 10: Ly teaches monitoring (**snooping**) using a checker to obtain an **output** from a circuit on semiconductor die via **simulation**. The checker further performs verification via simulated **input** to determine correct behavior (**desired output** check) of the circuit. (Abstract, Summary of Invention, Figs. 1, 2, 5, 6, CL2-L54, CL3-L1-7, CL3-L25, L50, CL25-L52) As previously mentioned, Ly also discloses that the use a **test case** (golden rule or test vector) in monitoring the operation of an integrated circuit simulation is well known. (see CL2-L18)*

*Regarding dependent claims 11-16: Ly discloses the steps of **checking** via an **interface** (**coupled** to) a monitor (for **snooping**) and automatically **generating** a checking sequence for use in **integrated circuit** design where the generator and checker are obviously **reusable**. (CL2-L54, CL3-L1-7, CL3-L25, L50, CL25-L52) Ly also teaches that the use a **test case** (golden rule or test vector) in monitoring the operation of an integrated circuit simulation is well known. (see CL2-L18)*

*Claims 17-23 are merely directed toward the computer readable medium and program instructions for the features outlined in claims 1-16 and are rejected using the reasoning as disclosed above.*

***Conclusion***

*4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.*

*U.S. Patent 6,157,972 issued to Newman et al teaches snooper use in ASIC design.*

*U.S. Patent 5,958,011 issued to Arimilli et al teaches circuit simulation and snooper use.*

*U.S. Patent 6,292,931 issued to Dupenloup teaches ASIC design monitoring and verification.*

*U.S. Patent 6,161,189 issued to Arimilli et al teaches latch and hold snooper circuit.*

*U.S. Patent 6,378,123 issued to Dupenloup teaches ASIC design simulation and verification.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.
Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.
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